Amendments to the Claims:

Please amend the claims as follows.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Currently Amended) A digital base booster (DBB) comprising:

an inputting portion including a plurality of multi-bit registers to respond to input data and first internal data;

a single data assigner including a single output for selecting one set of output data from a plurality of sets of output data of the inputting portion;

an arithmetic portion for performing an arithmetic operation on the output data of the data assigner and data stored in the arithmetic portion, compensating for a round-off error of the data output by the arithmetic operation, storing the compensated result and outputting the first internal data; and

an output data storing device for storing data processed in the arithmetic portion.

2. (Original) The digital base booster as claimed in claim 1, wherein one multi-bit register of the plurality of multi-bit registers stores the input data and outputs the stored input data in response to a related control signal, and the other multi-bit registers store the first internal data and output the stored first internal data in response to a related control signal.

3. (Original) The digital base booster as claimed in claim 1, wherein the data assigner is a multiplexer.

4. (Original) The digital base booster as claimed in claim 1, wherein the arithmetic portion comprises:

a first data register for storing second internal data;

a second data register for storing and outputting the output data of the data assigner;

a first multiplexer for selecting the output data of the first data register and the output data of the second data register;

an arithmetic data portion for selecting the output data of the data assigner and the second internal data to store and output intermediate data during an arithmetic operation;

an arithmetic processor for arithmetically processing the output data of the first multiplexer and data stored in the arithmetic processor, and adding the arithmetically-processed data to the output data of the arithmetic data portion to output the second internal data;

an error compensator for compensating for a round-off error for the second internal data which is the output data of the arithmetic processor; and

a third data register for storing the output data of the error compensator.

5. (Original) The digital base booster as claimed in claim 4, wherein the arithmetic data portion comprises:

a second multiplexer for selecting the second internal data and the output data of the data assigner;

a fourth data register for storing the output data of the second multiplexer; and

a data path controller for controlling transmission of the output data of the fourth data register.

6. (Original) The digital base booster as claimed in claim 4, wherein the arithmetic processor comprises:

a barrel shifter for performing an arithmetic operation in response to the output data of the first multiplexer;

a first adder for adding the output data of the barrel shifter; and

a second adder for adding the output data of the first adder to the output data of the arithmetic data portion.

7. (New) A digital base booster (DBB) comprising:

an inputting portion including a plurality of multi-bit registers to respond to input data and first internal data;

a data assigner for selecting one set of output data from a plurality of sets of output data of the inputting portion;

an arithmetic portion for performing an arithmetic operation on the output data of the data assigner and data stored in the arithmetic portion, compensating for a round-off error of the data output by the arithmetic operation, storing the compensated result and outputting the first internal data; and

an output data storing device for storing data processed in the arithmetic portion;

wherein the arithmetic portion comprises:

a first data register for storing second internal data;

a second data register for storing and outputting the output data of the data assigner;

a first multiplexer for selecting the output data of the first data register and the output data of the second data register;

an arithmetic data portion for selecting the output data of the data assigner and the second internal data to store and output intermediate data during an arithmetic operation;

an arithmetic processor for arithmetically processing the output data of the first multiplexer and data stored in the arithmetic processor, and adding the arithmetically-processed data to the output data of the arithmetic data portion to output the second internal data;

an error compensator for compensating for a round-off error for the second internal data which is the output data of the arithmetic processor; and

a third data register for storing the output data of the error compensator.

8. (New) The digital base booster as claimed in claim 7, wherein the arithmetic data portion comprises:

a second multiplexer for selecting the second internal data and the output data of the data assigner;

a fourth data register for storing the output data of the second multiplexer; and

a data path controller for controlling transmission of the output data of the fourth data register.

9. (New) The digital base booster as claimed in claim 7, wherein the arithmetic processor comprises:

a barrel shifter for performing an arithmetic operation in response to the output data of the first multiplexer;

a first adder for adding the output data of the barrel shifter; and

a second adder for adding the output data of the first adder to the output data of the arithmetic data portion.